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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,243	12/04/2003	Duck Young Jung	SUN-0035	7809

7590 02/01/2007

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EXAMINER	
PETERSON, CHRISTOPHER K	
ART UNIT	PAPER NUMBER
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/728,243	JUNG, DUCK YOUNG	
	Examiner	Art Unit	
	Christopher K. Peterson	2609	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file. However, the Korean Patent Application No. 2002-77099 document, filed Dec. 5, 2002, and United States Patent Application 10/72824, filed on Dec.4, 2003 do not match (for example, Figs. 1 – 6 of 2002-77099 are different from Figs. 1 – 6 of 10/728243). Date of foreign priority does not benefit until appropriate action is taken.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Arias-Estrada (US Patent #6253161).

As to claim 1, Arias-Estrada (Fig. 5) discloses an image sensor having a plurality of pixels (55), each pixel comprising: a photocell (photoreceptor 51) for receiving light and generating an analog signal corresponding to a quantity of the received light (Col. 6, lines 45-65 and Col. 11, lines 29-36); a comparator (Mp3 and Mp4 of Fig. 8) for comparing the analog signal of the photocell and a reference signal (Vref) and generating a digital signal having a value of the compared result (Col. 7, line 59 – Col. 8, line 16); and a switch (e.g. inverters provided in a non-retriggerable SRAM (45) are functioned as a switch) for outputting the digital signal of the comparator (Col. 8, line 43-65).

As to claim 15, Arias-Estrada teaches an optical pointing system comprising: a) a plurality of pixels, each having a photocell (photoreceptor 51) for receiving light and generating an analog signal corresponding to a quantity of the received light (Col. 6, lines 45-65 and Col. 11, lines 29-36), and a comparator (Mp3 and Mp4 of Fig. 8) for comparing the analog signal of the photocell and a reference signal (Vref) and generating a digital signal having a value of the compared result (Col. 7, line 59 – Col. 8, line 16); b) an image processor (digital module 40) for calculating a movement value using the digital signals outputted from the plurality of pixels (55) and generating a pixel select signal (sel_pix) and a shutter control information signal (sum_p); and c) a shutter control circuit (external circuitry) for generating a shutter control signal corresponding to the shutter control information signal of the image processor (Col. 9, line 20-34).

As to claim 2, Arias-Estrada teaches the image sensor as claimed in claim 1, wherein the digital signal is a digital signal having a 1-bit structure (i.e. 1 bit memory 45)(Col. 9, line 48 – 54).

As to claim 3, Arias-Estrada teaches the image sensor as claimed in claim 1, wherein the reference signal (Vref) is an analog signal of a photocell of an adjacent pixel (Col. 7, line 59 – Col. 8, line 16).

As to claim 4, Arias-Estrada teaches the image sensor as claimed in claim 1, wherein the reference signal is a reference voltage (Vref)(Col. 7, line 59 – Col. 8, line 16).

As to claim 5, Arias-Estrada teaches the image sensor as claimed in claim 1, wherein the photocell is a photo diode (51) that generates a photocurrent corresponding to the received quantity of light (Col. 6, line 44 - 53).

As to claim 6, Arias-Estrada teaches the image sensor as claimed in claim 1, wherein the comparator is a latch type comparator which outputs a first signal (e.g. high state signal such as 1) when the analog signal of the photocell is greater than the reference signal (Vref) and outputs a second signal (e.g. low state signal such as 0) when the analog signal of the photocell is less than the reference signal (Col. 8, line 4 – 11).

As to claim 16, Arias-Estrada teaches the optical pointing system as claimed in claim 15, wherein each of the plurality of pixels further comprises a switch (e.g. inverters provided in a non-retriggerable SRAM (45) are functioned as a switch) for outputting the digital signal of the comparator under the control of the pixel select signal (Col. 8, lines 43 – 65).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7 – 13 and 17 - 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arias-Estrada in view of Goto (US Patent 6982759).

As to claim 7, note the discussion of Arias-Estrada above, this claim differs from claim 1 only in that the limitation "second photocell" is additionally recited. Arias-Estrada does not teach wherein at least one second photocell for generating a second analog signal corresponding the received quantity of light. In same field of endeavor Goto (Fig. 1) teaches two photocells (1-1 and 1-2) at least a second photocell (1-2) for generating a second analog signal corresponding the received quantity of light. (Col. 2, lines 49 – 56). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a second photocell as taught by Goto to the pixel of Arias-Estrada because the second photocell allows the readout speed for one frame can be enhanced to twice the normal readout speed, thereby high speed operation is obtained. (Col. 5, line 54 – Col. 6, line 14 of Goto).

As to claim 17, note the discussion of Arias-Estrada and Goto above, this claim differs from claim 7 and 15 only in that the claim 15 has only one photodiode whereas claim 17 requires a second photodiode (Col. 2, lines 49 – 56 of Goto). Thus claim 17 is analyzed as previously discussed with respect to claim 15 and 7 above.

As to claim 8, Arias-Estrada teaches a digital signal having a 1-bit structure (i.e. 1 bit memory 45) (Col. 9, line 48 – 54 of Arias-Estrada).

As to claim 9, Arias-Estrada teaches the reference signal being an analog signal of an adjacent photocell of an adjacent pixel (Col. 7, line 59 – Col. 8, line 16).

As to claim 10, Arias-Estrada teaches the image sensor as claimed in claim 7, wherein the reference signal is a reference voltage (Col. 7, line 59 – Col. 8, line 16).

As to claim 11, Goto teaches above the image sensor as claimed in claim 7, wherein at least one of the first and second photocells comprises a photo diode (E.G. 1-2) and a transistor (2-2), the photodiode generating a photocurrent corresponding to the received quantity of light (Col. 2, line 57 - 65).

As to claim 12, Arias-Estrada teaches above the image sensor as claimed in claim 7, wherein the comparator is a latch type comparator which outputs a first signal when the analog signal of any one of the first and second photocells is greater than the reference signal and outputs a second signal when the analog signal of any one of the first and second photocells is less than the reference signal (Col. 8, line 4 -11).

As to claim 13, Goto teaches at least a second photocell (e.g. 1-2) is arranged inside each of the plurality of pixels. (Fig. 1 and Col. 2, lines 49 – 56).

As to claim 18 and 19 Arias-Estrada teaches the limitations of claims 18 and 19 as previously discussed with respect to claims 13 and 16 above, respectively since claims 18 and 19 recite the same limitations as claims 13 and 16.

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arias-Estrada in view of Goto, as applied to claim 7 above, and further in view of Sohn (US Patent 6365950).

As to claim 14, note the discussion of Arias-Estrada and Goto above, Arias-Estrada and Goto does not teach wherein the second photocell is arranged outside

each of the plurality of pixels. Sohn (Fig. 4) teaches at least a wherein the second photocell (122) is arranged outside each of the plurality of pixels. (Col. 4, lines 30 – 42 of Sohn). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a second photocell as taught by Sohn to the pixel of Arias-Estrada as modified by Goto because the second photocell allows better sensing efficiency of the sensor and image quality of the sensor are improved (Col. 5, line 22 – 32 of Sohn).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bock (US Patent # 6707410) is cited to teach a digital pixel sensor with a dynamic comparator having reduced threshold voltage sensitivity.

Martin (US Patent # 6271785) is cited to teach a CMOS imager with an A/D per pixel converter.

Castro (US Patent # 6590610) is cited to teach a digital double sampling in time integrating pixel sensors.

Knee (US Patent # 6963060) is cited to teach a photo-sensor array for motion detection.

Yamashita (US Patent # 6750437) is cited to teach an image pickup apparatus that suitably adjusts a focus.

Mizuno (US Patent # 6977682) is cited to teach a solid-state imaging device.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher K. Peterson whose telephone number is 571-270-1704. The examiner can normally be reached on Monday - Friday 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh D. Nguyen can be reached on 571-272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CKP

01/09/2007

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SUPERVISORY PATENT EXAMINER